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L4 and arithmetic and multiplexing and logic and shifter	3

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<u>L5</u>	L4 and arithmetic and multiplexing and logic and shifter	3	<u>L5</u>
<u>L4</u>	706/15-44.ccls.	2865	<u>L4</u>
<u>L3</u>	L1 and arithmetic and multiplexing and logic and shifter	0	<u>L3</u>
<u>L2</u>	L1 and arithmetic and multiplexing and logic and shifter and different near bit near sizing and different phases	407565	<u>L2</u>
<u>L1</u>	706/15.ccls.	355	<u>L1</u>

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☐ 1. Document ID: US 5263122 A

Using default format because multiple data bases are involved.

L5: Entry 1 of 3

File: USPT

Nov 16, 1993

US-PAT-NO: 5263122

DOCUMENT-IDENTIFIER: US 5263122 A

TITLE: Neural network architecture

DATE-ISSUED: November 16, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nunally; Patrick O.	Diamond Bar	CA		

US-CL-CURRENT: 706/41

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw D
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☐ 2. Document ID: US 5165010 A

L5: Entry 2 of 3

File: USPT

Nov 17, 1992

US-PAT-NO: 5165010

DOCUMENT-IDENTIFIER: US 5165010 A

TITLE: Information processing system

DATE-ISSUED: November 17, 1992

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Masuda; Noboru	Kokubunji			JP
Yasunaga; Moritoshi	Kawaguchi			JP
Yamada; Minoru	Hanno			JP
Masaki; Akira	Musashino			JP
Asai; Mitsuo	Kokubunji			JP
Hirai; Yuzo	Tsukuba			JP
Yagyu; Masayoshi	Kokubunji			JP
Hayashi; Takehisa	Kodaira			JP

Doi; Toshio Kokubunji JP  
Ishibashi; Kenichi Kokubunji JP

US-CL-CURRENT: 706/42

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMIC	Draw D
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☐ 3. Document ID: US 5138695 A

L5: Entry 3 of 3

File: USPT

Aug 11, 1992

US-PAT-NO: 5138695

DOCUMENT-IDENTIFIER: US 5138695 A

**\*\* See image for Certificate of Correction \*\***

TITLE: Systolic array image processing system

DATE-ISSUED: August 11, 1992

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Means; Robert W.	Rancho Santa Fe	CA		
Sklar; Horace J.	Escondido	CA		

US-CL-CURRENT: 706/41; 382/156, 382/278, 706/22

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMIC	Draw D
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arithmetic and multiplexing and logic and shifter and different near (bit-sizes or bit near sizes)	0

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<u>L8</u>	arithmetic and multiplexing and logic and shifter and different near (bit-sizes or bit near sizes)	0	<u>L8</u>
<u>L7</u>	L1 and arithmetic and multiplexing and logic and shifter and different near (bit-sizes or bit near sizes)	0	<u>L7</u>
<u>L6</u>	L5 and different near (bit-sizes or bit near sizes)	0	<u>L6</u>
<u>L5</u>	L4 and arithmetic and multiplexing and logic and shifter	3	<u>L5</u>
<u>L4</u>	706/15-44.ccls.	2865	<u>L4</u>
<u>L3</u>	L1 and arithmetic and multiplexing and logic and shifter	0	<u>L3</u>
<u>L2</u>	L1 and arithmetic and multiplexing and logic and shifter and different near bit near sizing and different phases	407565	<u>L2</u>
<u>L1</u>	706/15.ccls.	355	<u>L1</u>

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### Search Results -

Terms	Documents
L9 and arithmetic and neural and weights	0

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<u>L10</u>	L9 same different near phases	0	<u>L10</u>
<u>L9</u>	different near (bit-sizes or bit near sizes)	73	<u>L9</u>
<u>L8</u>	arithmetic and multiplexing and logic and shifter and different near (bit-sizes or bit near sizes)	0	<u>L8</u>
<u>L7</u>	L1 and arithmetic and multiplexing and logic and shifter and different near (bit-sizes or bit near sizes)	0	<u>L7</u>
<u>L6</u>	L5 and different near (bit-sizes or bit near sizes)	0	<u>L6</u>
<u>L5</u>	L4 and arithmetic and multiplexing and logic and shifter	3	<u>L5</u>
<u>L4</u>	706/15-44.ccls.	2865	<u>L4</u>
<u>L3</u>	L1 and arithmetic and multiplexing and logic and shifter	0	<u>L3</u>
<u>L2</u>	L1 and arithmetic and multiplexing and logic and shifter and different near bit near sizing and different phases	407565	<u>L2</u>

L1 706/15.ccls.

355 L1

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### Search Results -

Terms	Documents
L9 and different near phases	0

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<u>L12</u>	L9 and different near phases	0	<u>L12</u>
<u>L11</u>	L9 and arithmetic and neural and weights	0	<u>L11</u>
<u>L10</u>	L9 same different near phases	0	<u>L10</u>
<u>L9</u>	different near (bit-sizes or bit near sizes)	73	<u>L9</u>
<u>L8</u>	arithmetic and multiplexing and logic and shifter and different near (bit-sizes or bit near sizes)	0	<u>L8</u>
<u>L7</u>	L1 and arithmetic and multiplexing and logic and shifter and different near (bit-sizes or bit near sizes)	0	<u>L7</u>
<u>L6</u>	L5 and different near (bit-sizes or bit near sizes)	0	<u>L6</u>
<u>L5</u>	L4 and arithmetic and multiplexing and logic and shifter	3	<u>L5</u>
<u>L4</u>	706/15-44.ccls.	2865	<u>L4</u>
<u>L3</u>	L1 and arithmetic and multiplexing and logic and shifter	0	<u>L3</u>
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L2 bit near sizing and different phases

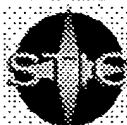
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L1 706/15.ccls.

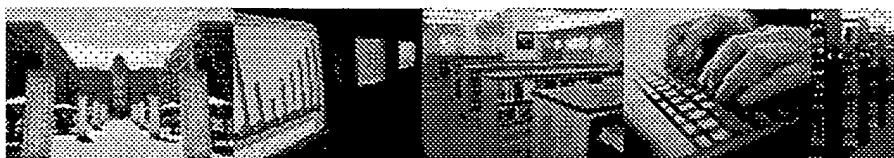
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IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

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- ☐ 1. **A bit-serial architecture for digital signal processing**  
Kanopoulos, N.;  
[Circuits and Systems, IEEE Transactions on](#)  
Volume 32, Issue 3, Mar 1985 Page(s):289 - 291  
[AbstractPlus](#) | Full Text: [PDF\(432 KB\)](#) IEEE JNL  
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- ☐ 2. **BER floors due to heterodyne coherent crosstalk in space photonic switch networks**  
Blumenthal, D.J.; Granstrand, P.; Thylen, L.;  
[Photonics Technology Letters, IEEE](#)  
Volume 8, Issue 2, Feb. 1996 Page(s):284 - 286  
Digital Object Identifier 10.1109/68.484268  
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- ☐ 3. **Digital phased array beamforming using single-bit delta-sigma conversion uniform oversampling**  
Kozak, M.; Karaman, M.;  
[Ultrasonics, Ferroelectrics and Frequency Control, IEEE Transactions on](#)  
Volume 48, Issue 4, July 2001 Page(s):922 - 931  
Digital Object Identifier 10.1109/58.935709  
[AbstractPlus](#) | Full Text: [PDF\(1684 KB\)](#) IEEE JNL  
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- ☐ 4. **Visualization of radiation-pattern characteristics of phased arrays using circular shifters**  
Clenet, M.; Morin, G.A.;  
[Antennas and Propagation Magazine, IEEE](#)  
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- ☐ 5. **Blind equalization of turbo trellis-coded partial-response continuous-phase signaling over narrow-band Rayleigh fading channels**  
Osman, O.; Ucan, O.N.;  
[Wireless Communications, IEEE Transactions on](#)

Volume 4, Issue 2, March 2005 Page(s):397 - 403  
Digital Object Identifier 10.1109/TWC.2004.840214

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- ☐ **6. Design of good low-density parity-check codes for block fading channels**  
Xiaowei Jin; Eckford, A.W.; Fuja, T.E.;  
[Military Communications Conference, 2004. MILCOM 2004. IEEE](#)  
Volume 2, 31 Oct.-3 Nov. 2004 Page(s):1054 - 1059 Vol. 2  
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IEE JNL IEE Journal or Magazine

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